ABSTRACT OF THE DISCLOSURE

A process for making an integrated circuit is described wherein sequence of mask steps is applied to a substrate or epitaxial layer of p-type material. The sequence consists of the following steps:

(1) applying a first mask and forming at least one N-well in said p-type material therethrough;

(2) applying a second mask and forming an active region therethrough;

(3) applying a third mask and forming a p-type field region therethrough;

(4) applying a fourth mask and forming a gate oxide therethrough;

(5) applying a fifth mask and carrying out a p-type implantation therethrough;

(6) applying a sixth mask and forming polysilicon gate regions therethrough;

(7) applying a seventh mask and forming a p-base region therethrough;

(8) applying an eighth mask and forming a N-extended region therethrough;

(9) applying a ninth mask and forming a p-top region therethrough;

(10) applying a tenth mask and carrying out an N+ implant therethrough;

(11) applying an eleventh mask and carrying out a P+ implant therethrough;

(12) applying a twelfth mask and forming contacts therethrough;

(13) applying a thirteenth mask and depositing a metal layer therethrough;

(14) applying a fourteenth mask and forming vias therethrough;

(15) applying a fifteenth mask and depositing a metal layer therethrough; and

(16) applying a sixteenth mask and forming a passivation layer therethrough. Up to any three of mask steps 4, 7, 8, and 9 may be omitted depending on the type of integrated circuit.